P24

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
HUYNH, KIM T

ART UNIT	PAPER NUMBER
2189	8

DATE MAILED: 06/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PPG

Office Action Summary	Application No.	Applicant(s)	
	09/583,883	LEE, TERRY R.	
	Examiner	Art Unit	
	Kim T. Huynh	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-14, 15-30, 31-44, 50-59, 65-72 are rejected under 35 U.S.C. 102(e) as being anticipated by Perino et al. (US Patent 6,545,875)

a. As per claim 1, 14, 30. Perino discloses method of routing a system bus to a plurality of expansion cards said method comprises:

- routing the bus (fig.3A, 25) into a first connector (fig.4, 51a) and into a first circuit card(fig.4, 41a) residing within the first connector; (col.5, lines 43-64), (col.6, lines 52-58)
- routing the bus from a portion of the first circuit card into a portion of a second circuit card residing within a second connector, wherein the bus is routed from the first circuit card to the second circuit card without entering the second connector; (fig.8), (col.6, lines 52-58)
- routing the bus through the second circuit card (fig.4, 41b) to the second connector (fig.4, 51b), (col.5, lines 43-64), (col.6, lines 52-58)

b. As per claim 4, 17, 33 Perino discloses the method further comprising the act of routing the bus out of the second connector (fig.4, 51c) into a portion of a system circuit board. (col.7, lines 32-43), (col.8, lines 20-27)

c. As per claim 5, 18. Perino discloses the method further comprising the act of terminating the bus after routing the bus out of the second connector. (col.5, lines 53-64)

d. As per claim 36, 51 Perino discloses a bus system comprising:

- a bus mounted on a circuit board of said system; (col.5, lines 43-54)
- a plurality of expansion slots (col.4, lines 40-41), each slot comprising a connector mounted on said circuit board (col.4, lines 56-59) and a circuit card residing within the connector, wherein said bus is routed into a first connector, into a first circuit card residing within said first connector, out of a portion of said first circuit card into a portion of a second circuit card residing within a second connector and through said second circuit card, and wherein said bus is routed from said first circuit card to said second circuit card without entering said second connector. (col.5, lines 43-54), (col.6, lines 52-58)

e. As per claims 2-3, 15-16, 31-32, 37-38, 52-53 Perino discloses bus routing 3rd to 4th card which inherently to claims 1, 30, 36 and 51 bus routing from 1st to 2nd card. (col.4, lines 40-41). (col.5, lines 43-54), (fig.8), (col.6, lines 52-58)

f. As per claim 21, 40 and 55, Perino discloses wherein said act of routing the bus from the portion of the first circuit card into the portion of the second circuit card comprises connecting the portion of the first circuit card to the portion of the second circuit card by a jumper mechanism. (col.6, lines 28-31)

g. As per claim 6,7 and 19, 20, 42, 57 Perino discloses the method wherein the first and second circuit cards each contain a top edge portion, each top edge portions being opposite an edge portion residing in a respective connector, arid wherein the bus is routed from the top edge portion of the first circuit card into the top edge portion of the second circuit card. (col.8, lines 65-67), (col.9, lines 1-23), (fig.8), (col.6, lines 25-37, 52-58)

h. As per claim 8 and 22, Perino discloses wherein said act of routing the bus from the portion of the first circuit card into the portion of the second circuit card comprises connecting the portion of the first circuit card to the portion of the second circuit card by a jumper mechanism. (col.6, lines 28-31)

i. As per claim 9, 23, Perino discloses wherein said act of routing the bus from the portion of the first circuit card into the portion of the second circuit card comprises connecting the portion of the first circuit card to the portion of the second circuit card by a circuit board having bus portion traces for continuing the bus between the first and second circuit cards. (col.6, lines 52-58), (col.6, lines 28-31), (fig.8)

j. As per claim 10, Perino discloses wherein said act of routing the bus from the portion of the first circuit card into the portion of the second circuit card comprises connecting the portion of the first circuit card to the portion of the second circuit card by a cable. (col.6, line 28-31), (col.6, lines 52-58)

k. As per claim 11-13, 24-26 Perino discloses wherein at least address, data and control signals are routed on said bus between the first and second circuit cards. (col.8, lines 37-41), (col.1, lines 19-26)

l. As per claim 27, Perino discloses wherein the bus is routed into the first circuit card (fig.4, 41a) by routing the bus into a first connector (fig.4, 51a) in which the first circuit card is residing. (col.5, lines 43-54)

m. As per claim 28, Perino discloses wherein the bus is routed out of the second circuit card (fig.4, 41b) by routing the bus out into a second connector in which the second circuit card is residing. (col.5, lines 43-54)

n. As per claim 29, Perino discloses wherein a first portion of bus (fig.4, 301) signals are routed between the first and second circuit cards and a second portion of bus signals are provided to the second circuit card from the motherboard (col.6, lines 28-31)

o. As per claim 66-68, 70 Perino discloses a processor-based system comprising:

- a processor; (col.5, lines 53-55), wherein bus system configured inherently discloses processing)

- a bus system (fig.9, 92) coupled to said processor; (col.5, lines 53-54), (col.7, lines 4-11)
- a bus mounted on a circuit board of said system; (col.6, lines 55-57)
- a plurality of expansion slots(col.4, lines 40-41), each slot comprising a connector mounted on said circuit board (col.4, lines 56-59) and a circuit card residing within the connector, wherein said bus is routed into a first connector, into a first circuit card residing within said first connector, out of a portion of said first circuit card into a portion of a second circuit card residing within a second connector, through said second circuit card and out of said second connector, wherein said bus is routed from said first circuit card into said second circuit card without entering said second connector. (col.6, lines 52-58), (col.6, lines 28-31), (fig.8)

p. As per claim 34, 71 Perino discloses wherein the bus is routed to a first interface device connected the device on the first circuit card and the first interface device provides bus signals to the device on the first circuit card. (col.5, lines 43-52), (col.6, lines 52-67)

q. As per claim 35, 72 Perino discloses wherein the bus is routed to a second interface device connected the device on the second circuit card and the second interface device provides bus signals to the device on the second circuit card. (col.5, lines 43-52), (col.6, lines 52-67)

r. As per claim 39, 54 Perino discloses wherein said bus is terminated by a plurality of resistors(col.5, lines 53-64)

s. As per claim 41, 56 Perino discloses wherein said portions are located at a top edge of said first and second circuit cards opposite a bottom edge residing in said connectors. (col.8, lines 65-67), (col.9, lines 1-23), (fig.8), (col.6, lines 25-37, 52-58)

t. As per claim 43, 58 Perino discloses wherein said jumper mechanism comprises:

- a circuit board having bus portion traces (col.5, lines 53-64) configured for continuing said bus between said first and second circuit cards; (col.7, lines 4-11)
- a plurality of connectors coupled to said circuit board, at least one connector adapted to receive said portion of said first circuit card and at least one other connector adapted to receive. said portion of said second circuit card. (fig.8), (col.6, lines 52-58)

u. As per claim 44, 59 Perino discloses wherein said jumper mechanism comprises:

- a cable configured for continuing said bus between said first and second circuit cards; (col.7, lines 4-11)
- a plurality of connectors coupled to said cable, at least one connector adapted to receive said portion of said first circuit card and at least one other connector adapted to receive said portion of said second circuit card. (col.6, lines 52-58)

v. As per claim 50, 65 Perino discloses wherein said circuit cards are dynamic random access memory circuit cards and said system further comprises a memory controller coupled to said bus. (col.5, lines 24-26)

w. As per claim 69, Perino discloses a circuit card for use in a expandable system comprising:

- an input bus connection for receiving signals from a system bus; (col.5, lines 43-64)
- an output bus connection for outputting signals to said bus; (col.5, lines 43-64)
- a bus portion connecting said input bus connection to said output bus connection for routing bus signals through said card, wherein either said input bus connection does not connect to a connector in which said card resides or said output bus connection does not connect to a connector in which said card resides. (col.6, lines 52-58), (col.6, lines 28-31), (fig.8)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 45 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino et al. (US Patent 6,545,875) in view of Cargin, Jr. et al. (U.S Patent 6,023,147)

Perino discloses the limitation of connection circuits via bus cable except Perino fails to disclose specific type of cable as claimed in claims 45 and 60, the ribbon cable. However, Cargin discloses ribbon cable, (col.17, lines 21-29) It would have been obvious one having ordinary skills in the art at the time the invention was made to incorporate Cargin's teaching into Perino's method to have a ribbon cable which the equivalent purpose of transmitting digital data between devices.

5. Claims 46-49 and 61-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino et al. (US Patent 6,545,875) in view of Handbook of LAN Cable Testing, Wavetek

Perino discloses the limitation of connection circuits via bus cable except Perino fails to disclose specific type of cable as claimed in claims 46-49 and 61-64, ribbon cable with a shield , coaxial cable, a twisted pair wiring and a waveguide. However, the Handbook of Lan Cable Testing discloses different types of cable which included shied/unshield, coaxial cable, a twisted pair wiring and a waveguide. (see page 55-56)

It would have been obvious one having ordinary skills in the art at the time the invention was made to incorporate different types of cable into Perino's method to have a variety of cable which the equivalent purpose of transmitting digital data between devices.

Response to Arguments

6. Applicant's arguments filed on 4/9/03 have been considered but are moot in view of the new ground(s) of rejection.

In response to applicant's argument that Apel's reference does not disclose the method of routing system bus to a plurality of cards. However, Perino discloses the module to module(card) connection continue by bus system, the system is complete when last module terminated. (col.5, lines 53-55), (fig.8, col.6, lines 52-67), wherein bus route from module 81a to 81b.)

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sanwo et al. [USPN 5,530,623] discloses connections

Gillespie et al. [USPN 5,835,784] discloses expansion chassis

8. A shortened statutory period for reply is set to expire THREE months from the mailing date of this communication. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) months from the mailing date of this communication. If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) months from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM-6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7249 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

June 13, 2003

RUPAL DHARIA
PRIMARY EXAMINER